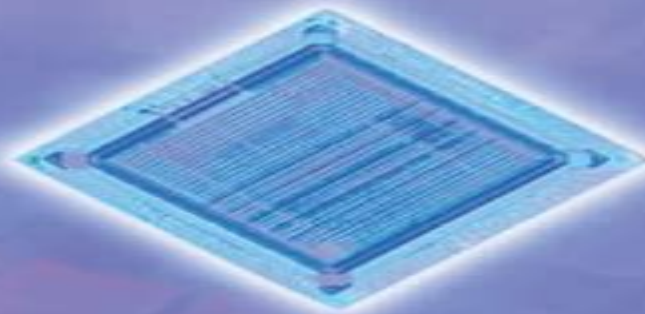


Low Power Methodology Manual

For System-on-Chip Design



Michael Keating David Flynn
Robert Aitken Alan Gibbons Kaijian Shi

 **Springer**

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Low Power Methodology Manual David Flynn, Rob Aitken, Alan Gibbons, Kaijian Shi, 2007-07-31 Tools alone aren't enough to reduce dynamic and leakage power in complex chip designs a well planned methodology is needed Following in the footsteps of the successful Reuse Methodology Manual RMM authors from ARM and Synopsys have written this Low Power Methodology Manual LPMM to describe such a low power methodology with a practical step by step approach Richard Goering Software Editor EE Times Excellent compendium of low power techniques and guidelines with balanced content spanning theory and practical implementation The LPMM is a very welcome addition to the field of low power SoC implementation that has for many years operated in a largely ad hoc fashion Sujeeth Joseph Chief Architect Semiconductor and Systems Solutions Unit Wipro Technologies The LPMM enables broader adoption of aggressive power management techniques based on extensive experience and silicon example with real data that every SOC designer can use to meet the difficulties faced in managing the power issues in deep submicron designs Anil Mankar Sr VP Worldwide Core Engineering and Chief Development Officer Conexant Systems Inc Managing power at 90nm and below introduces significant challenges to design flow The LPMM is a timely and immediately useful book that shows how combination of tools IP and methodology can be used together to address power management Nick Salter Head of Chip Integration CSR plc

Low Power Methodology Manual David Flynn, Rob Aitken, Alan Gibbons, Kaijian Shi, 2007-12-19 This book provides a practical guide for engineers doing low power System on Chip SoC designs It covers various aspects of low power design from architectural issues and design techniques to circuit design of power gating switches In addition to providing a theoretical basis for these techniques the book addresses the practical issues of implementing them in today's designs with today's tools Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Jose L. Ayala, Braulio

Garcia-Camara, Manuel Prieto, Martino Ruggiero, Gilles Sicard, 2011-09-15 This book constitutes the refereed proceedings of the 21st International Conference on Integrated Circuit and System Design PATMOS 2011 held in Madrid Spain in September 2011 The 34 revised full papers presented were carefully reviewed and selected from numerous submissions The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems and focus especially on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling design characterization analysis and optimization

Introduction to Low-Power Design in VLSIs Patrick Lee, 2011-12-12 This book discusses one increasingly important issue in the VLSI design low power It covers the following topics a basic concepts of low power design b low power design methods and applications in industry chips and c commercial CAD tools on low power design This book discusses the concepts a set of known methods industry cases and CAD tools on the low power design It is organized in four chapters and a glossary is provided at the end of the book

Low-Power VLSI Circuits and Systems Ajit Pal, 2014-11-17 The book provides a comprehensive coverage of

different aspects of low power circuit synthesis at various levels of design hierarchy starting from the layout level to the system level For a seamless understanding of the subject basics of MOS circuits has been introduced at transistor gate and circuit level followed by various low power design methodologies such as supply voltage scaling switched capacitance minimization techniques and leakage power minimization approaches The content of this book will prove useful to students researchers as well as practicing engineers Introduction to VLSI Systems Ming-Bo Lin,2011-11-28 With the advance of semiconductors and ubiquitous computing the use of system on a chip SoC has become an essential technique to reduce product cost With this progress and continuous reduction of feature sizes and the development of very large scale integration VLSI circuits addressing the harder problems requires fundamental understanding *Low-Power Wireless Communication Circuits and Systems* Kiat Seng Yeo,Kaixue Ma,2018-05-03 The increasing demand for extremely high data rate communications has urged researchers to develop new communication systems Currently wireless transmission with more than one Giga bits per second Gbps data rates is becoming essential due to increased connectivity between different portable and smart devices To realize Gbps data rates millimeter wave MMW bands around 60 GHz is attractive due to the availability of large bandwidth of 9 GHz Recent research work in the Gbps data rates around 60 GHz band has focused on short range indoor applications such as uncompressed video transfer high speed file transfer between electronic devices and communication to and from kiosk Many of these applications are limited to 10 m or less because of the huge free space path loss and oxygen absorption for 60 GHz band MMW signal This book introduces new knowledge and novel circuit techniques to design low power MMW circuits and systems It also focuses on unlocking the potential applications of the 60 GHz band for high speed outdoor applications The innovative design application significantly improves and enables high data rate low cost communication links between two access points seamlessly The 60 GHz transceiver system on chip provides an alternative solution to upgrade existing networks without introducing any building renovation or external network laying works

Design and Modeling of Low Power VLSI Systems Sharma, Manoj,Gautam, Ruchi,Khan, Mohammad Ayoub,2016-06-06 Very Large Scale Integration VLSI Systems refer to the latest development in computer microchips which are created by integrating hundreds of thousands of transistors into one chip Emerging research in this area has the potential to uncover further applications for VSLI technologies in addition to system advancements Design and Modeling of Low Power VLSI Systems analyzes various traditional and modern low power techniques for integrated circuit design in addition to the limiting factors of existing techniques and methods for optimization Through a research based discussion of the technicalities involved in the VLSI hardware development process cycle this book is a useful resource for researchers engineers and graduate level students in computer science and engineering *Integrated Circuit and System Design. Power and Timing Modeling, Optimization, and Simulation* Rene van Leuken,Gilles Sicard,2011-02-04 This book constitutes the refereed proceedings of the 20th International Conference on Integrated Circuit and System Design PATMOS 2010 held in Grenoble

France in September 2010 The 24 revised full papers presented and the 9 extended abstracts were carefully reviewed and are organized in topical sections on design flows circuit techniques low power circuits self timed circuits process variation high level modeling of poweraware heterogeneous designs in SystemC AMS and minalogic

Integrated Circuit and System Design: Power and Timing Modeling, Optimization and Simulation José Monteiro, Rene van

Leuken, 2010-02-06 This book constitutes the thoroughly refereed post conference proceedings of 19th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2009 featuring Integrated Circuit and System Design held in Delft The Netherlands during September 9 11 2009 The 26 revised full papers and 10 revised poster papers presented were carefully reviewed and selected from numerous submissions The papers are organized in topical sections on variability statistical timing circuit level techniques power management low power circuits technology system level techniques power timing optimization techniques self timed circuits low power circuit analysis optimization and low power design studies

Low Power Circuits for Emerging Applications in Communications, Computing, and Sensing Fei Yuan, 2018-12-07 The book addresses the need to investigate new approaches to lower energy requirement in multiple application areas and serves as a guide into emerging circuit technologies It explores revolutionary device concepts sensors and associated circuits and architectures that will greatly extend the practical engineering limits of energy efficient computation The book responds to the need to develop disruptive new system architectures circuit microarchitectures and attendant device and interconnect technology aimed at achieving the highest level of computational energy efficiency for general purpose computing systems Features Discusses unique technologies and material only available in specialized journal and conferences Covers emerging applications areas such as ultra low power communications emerging bio electronics and operation in extreme environments Explores broad circuit operation ex analog RF memory and digital circuits Contains practical applications in the engineering field as well as graduate studies Written by international experts from both academia and industry

Low Power Design Essentials Jan Rabaey, 2009-04-21 Low Power Design Essentials contains all the topics of importance to the low power designer The book lays the foundation with background chapters entitled Advanced MOS Transistors and Their Models and Power Basics These chapters are followed by chapters on the design process including optimization architecture and algorithm level memory run time standby logic and standby memory Chapters on special topics are also included power management and modal design ultra low power and low power design methodology and flows The book concludes with a chapter on case studies as well as a chapter on Projection into the Future These chapters are all based on the extensive amount of teaching that the author has carried out both at universities and companies worldwide All chapters have been drawn up specifically for self study They aim however at different levels of understanding All the chapters start with elementary material but most also contain advanced material

Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology Luciano Lavagno, Igor L.

Markov, Grant Martin, Louis K. Scheffer, 2017-02-03 The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic RTL to GDSII a file format used to transfer data of semiconductor physical layout design flow analog mixed signal design physical verification and technology computer aided design TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability DFM at the nanoscale power supply network design and analysis design modeling and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity Electronic Design Automation for IC Implementation Circuit Design and Process Technology provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals **Dynamic Modelling** Alisson Brito, 2010-01-01 When talking about modelling it is natural to talk about simulation Simulation is the imitation of the operation of a real world process or systems over time The objective is to generate a history of the model and the observation of that history helps us understand how the real world system works not necessarily involving the real world into this process A system or process model takes the form of a set of assumptions concerning its operation In a model mathematical and logical assumptions are considered and entities and their relationship are delimited The objective of a model and its respective simulation is to answer a vast number of what if questions Some questions answered in this book are What if the power distribution system does not work as expected What if the produced ships were not able to transport all the demanded containers through the Yangtze River in China And what if an installed wind farm does not produce the expected amount of energyt Answering these questions without a dynamic simulation model could be extremely expensive or even impossible in some cases and this book aims to present possible solutions to these problems *Handbook of Energy-Aware and Green Computing - Two Volume Set* Ishfaq Ahmad, Sanjay Ranka, 2016-02-03 Implementing energy efficient CPUs and peripherals as well as reducing resource consumption have become emerging trends in computing As computers increase in speed and power their energy issues become more and more prevalent The need to develop and promote environmentally friendly computer technologies and systems has also come to the forefront *Handbook of Energy-Aware and Green Computing, Volume 2* Ishfaq Ahmad, Sanjay Ranka, 2013-01-31 This book provides basic and fundamental knowledge of various aspects of energy aware computing at the component software and system level It provides a broad range of topics dealing with power energy and temperature related research areas for individuals from industry and academia Dual Mode Logic Itamar

Levi,Alexander Fish,2020-12-15 This book presents Dual Mode Logic DML a new design paradigm for digital integrated circuits DML logic gates can operate in two modes each optimized for a different metric Its on the fly switching between these operational modes at the gate block and system levels provide maximal E D optimization flexibility Each highly detailed chapter has multiple illustrations showing how the DML paradigm seamlessly implements digital circuits that dissipate less energy while simultaneously improving performance and reducing area without a significant compromise in reliability All the facets of the DML methodology are covered starting from basic concepts through single gate optimization general module optimization design trade offs and new ways DML can be integrated into standard design flows using standard EDA tools DML logic is compatible with numerous applications but is particularly advantageous for ultra low power reliable high performance systems and advanced scaled technologies Written in language accessible to students and design engineers each topic is oriented toward immediate application by all those interested in an alternative to CMOS logic Describes a novel promising alternative to conventional CMOS logic known as Dual Mode Logic DML with which a single gate can be operated selectively in two modes each optimized for a different metric e g energy consumption performance size Demonstrates several techniques at the architectural level which can result in high energy savings and improved system performance Focuses on the tradeoffs between power area and speed including optimizations at the transistor and gate level including alternatives to DML basic cells Illustrates DML efficiency for a variety of VLSI applications An ASIC Low Power Primer

Rakesh Chadha,J. Bhasker,2012-12-05 This book provides an invaluable primer on the techniques utilized in the design of low power digital semiconductor devices Readers will benefit from the hands on approach which starts from the ground up explaining with basic examples what power is how it is measured and how it impacts on the design process of application specific integrated circuits ASICs The authors use both the Unified Power Format UPF and Common Power Format CPF to describe in detail the power intent for an ASIC and then guide readers through a variety of architectural and implementation techniques that will help meet the power intent From analyzing system power consumption to techniques that can be employed in a low power design to a detailed description of two alternate standards for capturing the power directives at various phases of the design this book is filled with information that will give ASIC designers a competitive edge in low power design **VLSI Design**

Esteban Tlelo-Cuautle,Sheldon X.-D. Tan,2012-01-20 This book provides some recent advances in design nanometer VLSI chips The selected topics try to present some open problems and challenges with important topics ranging from design tools new post silicon devices GPU based parallel computing emerging 3D integration and antenna design The book consists of two parts with chapters such as VLSI design for multi sensor smart systems on a chip Three dimensional integrated circuits design for thousand core processors Parallel symbolic analysis of large analog circuits on GPU platforms Algorithms for CAD tools VLSI design A multilevel memetic algorithm for large SAT encoded problems etc

Ultra Low Power ECG Processing System for IoT Devices Temesghen Tekeste Habte,Hani Saleh,Baker

Mohammad, Mohammed Ismail, 2018-09-06 This book describes an ECG processing architecture that guides biomedical SoC developers from theory to implementation and testing The authors provide complete coverage of the digital circuit implementation of an ultra low power biomedical SoC comprised of a detailed description of an ECG processor implemented and fabricated on chip Coverage also includes the challenges and tradeoffs of designing ECG processors Describes digital circuit architecture for implementing ECG processing algorithms on chip Includes coverage of signal processing techniques for ECG processing Features ultra low power circuit design techniques Enables design of ECG processing architectures and their respective on chip implementation

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