

241.

```

module circuit_4_51(X, F);
    module circuit_4_51(X);
        input [2:0] input F;
        output F;

        wire [0:4] wire [0:4] T;

        rand
            g0: T[0] = X[0] & X[1];
            g1: T[1] = X[0] & X[2];
            g2: T[2] = X[1] & X[2];
            g3: T[3] = X[0] & X[3];
            g4: T[4] = X[1] & X[2];
            g5: T[5] = X[2] & X[3];
    endmodule
endmodule

```

# Logic Instructors Solution Manual

**Jin-Ying Zhang**



## **Logic Instructors Solution Manual:**

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