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Low Power Design with High-Level Power Estimation and Power-Aware Synthesis

Springer

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Massoud Pedram,Jan M. Rabaey

Low Power Design With High Level Power Estimation And Power Aware Synthesis:

Low Power Design with High-Level Power Estimation and Power-Aware Synthesis ,2011-10-22 **Low Power Design with High-Level Power Estimation and Power-Aware Synthesis** Sumit Ahuja,Avinash Lakshminarayana,Sandeep Kumar Shukla,2011-10-22 This book presents novel research techniques algorithms methodologies and experimental results for high level power estimation and power aware high level synthesis Readers will learn to apply such techniques to enable design flows resulting in shorter time to market and successful low power ASIC FPGA design Low Power Hardware Synthesis from Concurrent Action-Oriented Specifications Gaurav Singh,Sandeep Kumar Shukla,2010-07-23 Human lives are getting increasingly entangled with technology especially comp ing and electronics At each step we take especially in a developing world we are dependent on various gadgets such as cell phones handheld PDAs netbooks me cal prosthetic devices and medical measurement devices e g blood pressure m itors glucometers Two important design constraints for such consumer electronics are their form factor and battery life This translates to the requirements of reduction in the die area and reduced power consumption for the semiconductor chips that go inside these gadgets Performance is also important as increasingly sophisticated applications run on these devices and many of them require fast response time The form factor of such electronics goods depends not only on the overall area of the chips inside them but also on the packaging which depends on thermal ch acteristics Thermal characteristics in turn depend on peak power signature of the chips As a result while the overall energy usage reduction increases battery life peak power reduction in uences the form factor One more important aspect of these electronic equipments is that every 6 months or so a newer feature needs to be added to keep ahead of the market competition and hence new designs have to be completed with these new features better form factor battery life and performance every few months This extreme pressure on the time to market is another force that drives the innovations in design automation of semiconductor chips *Low-Power Electronics Design* Christian Piguet,2018-10-03 The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high performance chips and portable devices The study of power saving design methodologies now must also include subjects such as systems on chips embedded software and the future of microelectronics Low Power Electronics Design covers all major aspects of low power design of ICs in deep submicron technologies and addresses emerging topics related to future design This volume explores in individual chapters written by expert authors the many low power techniques born during the past decade It also discusses the many different domains and disciplines that impact power consumption including processors complex circuits software CAD tools and energy sources and management The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality They investigate nanotechnologies optical circuits ad hoc networks e textiles as well as human powered sources of energy Low Power Electronics Design delivers a complete picture of today s methods for reducing power and also illustrates the advances in

chip design that may be commonplace 10 or 15 years from now *On-Chip Communication Architectures* Sudeep Pasricha,Nikil Dutt,2010-07-28 Over the past decade system on chip SoC designs have evolved to address the ever increasing complexity of applications fueled by the era of digital convergence Improvements in process technology have effectively shrunk board level components so they can be integrated on a single chip New on chip communication architectures have been designed to support all inter component communication in a SoC design These communication architecture fabrics have a critical impact on the power consumption performance cost and design cycle time of modern SoC designs As application complexity strains the communication backbone of SoC designs academic and industrial R D efforts and dollars are increasingly focused on communication architecture design On Chip Communication Architecures is a comprehensive reference on concepts research and trends in on chip communication architecture design It will provide readers with a comprehensive survey not available elsewhere of all current standards for on chip communication architectures A definitive guide to on chip communication architectures explaining key concepts surveying research efforts and predicting future trends Detailed analysis of all popular standards for on chip communication architectures Comprehensive survey of all research on communication architectures covering a wide range of topics relevant to this area spanning the past several years and up to date with the most current research efforts Future trends that with have a significant impact on research and design of communication architectures over the next several years **Low-Power High-Level Synthesis for Nanoscale CMOS Circuits** Saraju P. Mohanty,Nagarajan Ranganathan,Elias Kougianos,Priyardarsan Patra,2008-05-31 Low Power High Level Synthesis for Nanoscale CMOS Circuits addresses the need for analysis characterization estimation and optimization of the various forms of power dissipation in the presence of process variations of nano CMOS technologies The authors show very large scale integration VLSI researchers and engineers how to minimize the different types of power consumption of digital circuits The material deals primarily with high level architectural or behavioral energy dissipation because the behavioral level is not as highly abstracted as the system level nor is it as complex as the gate transistor level At the behavioral level there is a balanced degree of freedom to explore power reduction mechanisms the power reduction opportunities are greater and it can cost effectively help in investigating lower power design alternatives prior to actual circuit layout or silicon implementation The book is a self contained low power high level synthesis text for Nanoscale VLSI design engineers and researchers Each chapter has simple relevant examples for a better grasp of the principles presented Several algorithms are given to provide a better understanding of the underlying concepts The initial chapters deal with the basics of high level synthesis power dissipation mechanisms and power estimation In subsequent parts of the text a detailed discussion of methodologies for the reduction of different types of power is presented including Power Reduction Fundamentals Energy or Average Power Reduction Peak Power Reduction Transient Power Reduction Leakage Power Reduction Low Power High Level Synthesis for Nanoscale CMOS Circuits provides a valuable resource for the design of low

power CMOS circuits **Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation** Jorge Juan Chico,Enrico Macii,2003-10-02 Welcome to the proceedings of PATMOS 2003 This was the 13th in a series of international workshops held in several locations in Europe Over the years PATMOS has gained recognition as one of the major European events devoted to power and timing aspects of integrated circuit and system design Despite its signi cant growth and development PATMOS can still be considered as a very informal forum featuring high level scienti c presentations together with open discussions and panel sessions in a free and relaxed environment This year PATMOS took place in Turin Italy organized by the Politecnico di Torino with technical co sponsorship from the IEEE Circuits and Systems Society and the generous support of the European Commission as well as that of several industrial sponsors including BullDAST Cadence Mentor Graphics STMicroelectronics and Synopsys The objective of the PATMOS workshop is to provide a forum to discuss and investigate the emerging problems in methodologies and tools for the design of new generations of integrated circuits and systems A major emphasis of the technical program is on speed and low power aspects with particular regard to modeling characterization design and architectures *Power Aware Computing* Robert Graybill,Rami Melhem,2013-04-17 With the advent of portable and autonomous computing systems power con sumption has emerged as a focal point in many research projects commercial systems and DoD platforms One current research initiative which drew much attention to this area is the Power Aware Computing and Communications PAC C program sponsored by DARPA Many of the chapters in this book include results from work that have been supported by the PACIC program The performance of computer systems has been tremendously improving while the size and weight of such systems has been constantly shrinking The capacities of batteries relative to their sizes and weights has been also improv ing but at a rate which is much slower than the rate of improvement in computer performance and the rate of shrinking in computer sizes The relation between the power consumption of a computer system and it performance and size is a complex one which is very much dependent on the specific system and the technology used to build that system We do not need a complex argument however to be convinced that energy and power which is the rate of energy consumption are becoming critical components in computer systems in gen eral and portable and autonomous systems in particular Most of the early research on power consumption in computer systems ad dressed the issue of minimizing power in a given platform which usually translates into minimizing energy consumption and thus longer battery life **Power-Aware Architecting** Maarten Ditzel,R.H. Otten,Wouter A. Serdijn,2007-10-11 Thecomplexityofembeddedsystems on a chipisrapidlygrowing Di erentexpertsareinvolvedin the design process application software designers programmable core architects on chip com nication engineers analog and digital designers deep submicron specialists and process engineers In order to arrive at an optimum implementation compromises are needed across boundaries of the di erent domains of expertise Therefore the authors of this book take the point of view of the system architect who is a generalist rather than an expert He is responsible for the de nition of a high level architecture

whichisgloballyoptimal Findinganoptimumrequiresaproperbalancebetweenarea performance and last but not least energy consumption The challenge is not only the size of the design space but also the fact that the most important decisions are taken during the early design phases The advantage of an early decision is that the impact on area performance and energy consumption is large But the disadvantage is that the available information is often limited incomplete and inaccurate The task of the system architect is to take the correct early decisions despite the uncertainties *Languages, Design Methods, and Tools for Electronic System Design* Frank Oppenheimer,Julio Luis Medina Pasaje,2015-12-11 This book brings together a selection of the best papers from the seventeenth edition of the Forum on specification and Design Languages Conference FDL which took place on October 14 16 2014 in Munich Germany FDL is a well established international forum devoted to dissemination of research results practical experiences and new ideas in the application of specification design and verification languages to the design modeling and verification of integrated circuits complex hardware software embedded systems and mixed technology systems Power Aware Design Methodologies Massoud Pedram,Jan M. Rabaey,2007-05-08 Power Aware Design Methodologies was conceived as an effort to bring all aspects of power aware design methodologies together in a single document It covers several layers of the design hierarchy from technology circuit logic and architectural levels up to the system layer It includes discussion of techniques and methodologies for improving the power efficiency of CMOS circuits digital and analog systems on chip microelectronic systems wirelessly networked systems of computational nodes and so on In addition to providing an in depth analysis of the sources of power dissipation in VLSI circuits and systems and the technology and design trends this book provides a myriad of state of the art approaches to power optimization and control The different chapters of Power Aware Design Methodologies have been written by leading researchers and experts in their respective areas Contributions are from both academia and industry The contributors have reported the various technologies methodologies and techniques in such a way that they are understandable and useful **Low-Power CMOS Circuits** Christian Piguet,2018-10-03 The power consumption of microprocessors is one of the most important challenges of high performance chips and portable devices In chapters drawn from Piguet s recently published Low Power Electronics Design Low Power CMOS Circuits Technology Logic Design and CAD Tools addresses the design of low power circuitry in deep submicron technologies It provides a focused reference for specialists involved in designing low power circuitry from transistors to logic gates The book is organized into three broad sections for convenient access The first examines the history of low power electronics along with a look at emerging and possible future technologies It also considers other technologies such as nanotechnologies and optical chips that may be useful in designing integrated circuits The second part explains the techniques used to reduce power consumption at low levels These include clock gating leakage reduction interconnecting and communication on chips and adiabatic circuits The final section discusses various CAD tools for designing low power circuits This section includes three chapters that demonstrate the tools and low power design issues at three major

companies that produce logic synthesizers Providing detailed examinations contributed by leading experts Low Power CMOS Circuits Technology Logic Design and CAD Tools supplies authoritative information on how to design and model for high performance with low power consumption in modern integrated circuits It is a must read for anyone designing modern computers or embedded systems **Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology** Luciano Lavagno,Igor L. Markov,Grant Martin,Louis K. Scheffer,2017-02-03 The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook Second Edition Electronic Design Automation for IC Implementation Circuit Design and Process Technology thoroughly examines real time logic RTL to GDSII a file format used to transfer data of semiconductor physical layout design flow analog mixed signal design physical verification and technology computer aided design TCAD Chapters contributed by leading experts authoritatively discuss design for manufacturability DFM at the nanoscale power supply network design and analysis design modeling and much more New to This Edition Major updates appearing in the initial phases of the design flow where the level of abstraction keeps rising to support more functionality with lower non recurring engineering NRE costs Significant revisions reflected in the final phases of the design flow where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting edge applications and approaches realized in the decade since publication of the previous edition these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity Electronic Design Automation for IC Implementation Circuit Design and Process Technology provides a valuable state of the art reference for electronic design automation EDA students researchers and professionals

Multi-Core Embedded Systems Georgios Kornaros,2018-10-08 Details a real world product that applies a cutting edge multi core architecture Increasingly demanding modern applications such as those used in telecommunications networking and real time processing of audio video and multimedia streams require multiple processors to achieve computational performance at the rate of a few giga operations per second This necessity for speed and manageable power consumption makes it likely that the next generation of embedded processing systems will include hundreds of cores while being increasingly programmable blending processors and configurable hardware in a power efficient manner Multi Core Embedded Systems presents a variety of perspectives that elucidate the technical challenges associated with such increased integration of homogeneous processors and heterogeneous multiple cores It offers an analysis that industry engineers and professionals will need to understand the physical details of both software and hardware in embedded architectures as well as their limitations and potential for future growth Discusses the available programming models spread across different abstraction levels The book begins with an overview of the evolution of multiprocessor architectures for embedded applications and discusses techniques for autonomous power management of system level parameters It addresses the use of existing open source and free tools originating from several application domains such as traffic modeling graph theory

parallel computing and network simulation In addition the authors cover other important topics associated with multi core embedded systems such as Architectures and interconnects Embedded design methodologies Mapping of applications

Multiprocessor System-on-Chip Michael Hübner,Jürgen Becker,2010-11-25 The purpose of this book is to evaluate strategies for future system design in multiprocessor system on chip MPSoC architectures Both hardware design and integration of new development tools will be discussed Novel trends in MPSoC design combined with reconfigurable architectures are a main topic of concern The main emphasis is on architectures design flow tool development applications and system design Proceedings of the 1st International Conference on Electronic Engineering and Renewable Energy Bekkay Hajji,Giuseppe Marco Tina,Kamal Ghoumid,Abdelhamid Rabhi,Adel Mellit,2018-08-01 The proceedings present a selection of refereed papers presented at the 1st International Conference on Electronic Engineering and Renewable Energy ICEERE 2018 held during 15 17 April 2018 Saidi Morocco The contributions from electrical engineers and experts highlight key issues and developments essential to the multifaceted field of electrical engineering systems and seek to address multidisciplinary challenges in Information and Communication Technologies The book has a special focus on energy challenges for developing the Euro Mediterranean regions through new renewable energy technologies in the agricultural and rural areas The book is intended for academia including graduate students experienced researchers and industrial practitioners working in the fields of Electronic Engineering and Renewable Energy *Green Mobile Devices and Networks* Hrishikesh Venkataraman,Gabriel-Miro Muntean,2016-04-19 While battery capacity is often insufficient to keep up with the power demanding features of the latest mobile devices powering the functional advancement of wireless devices requires a revolution in the concept of battery life and recharge capability Future handheld devices and wireless networks should be able to recharge themselves automaticall *System-Level Design Techniques for Energy-Efficient Embedded Systems* Marcus T. Schmitz,Bashir M. Al-Hashimi,Petru Eles,2006-01-16 System Level Design Techniques for Energy Efficient Embedded Systems addresses the development and validation of co synthesis techniques that allow an effective design of embedded systems with low energy dissipation The book provides an overview of a system level co design flow illustrating through examples how system performance is influenced at various steps of the flow including allocation mapping and scheduling The book places special emphasis upon system level co synthesis techniques for architectures that contain voltage scalable processors which can dynamically trade off between computational performance and power consumption Throughout the book the introduced co synthesis techniques which target both single mode systems and emerging multi mode applications are applied to numerous benchmarks and real life examples including a realistic smart phone

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Johan Vounckx,Nadine Azemard,Philippe Maurine,2006-09-07 This book constitutes the refereed proceedings of the 16th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2006 The book presents 41

revised full papers and 23 revised poster papers together with 4 key notes and 3 industrial abstracts Topical sections include high level design power estimation and modeling memory and register files low power digital circuits busses and interconnects low power techniques applications and SoC design modeling and more *Low-Power Processors and Systems on Chips* Christian Piguet,2018-10-03 The power consumption of microprocessors is one of the most important challenges of high performance chips and portable devices In chapters drawn from Piguet s recently published Low Power Electronics Design this volume addresses the design of low power microprocessors in deep submicron technologies It provides a focused reference for specialists involved in systems on chips from low power microprocessors to DSP cores reconfigurable processors memories ad hoc networks and embedded software Low Power Processors and Systems on Chips is organized into three broad sections for convenient access The first section examines the design of digital signal processors for embedded applications and techniques for reducing dynamic and static power at the electrical and system levels The second part describes several aspects of low power systems on chips including hardware and embedded software aspects efficient data storage networks on chips and applications such as routing strategies in wireless RF sensing and actuating devices The final section discusses embedded software issues including details on compilers retargetable compilers and coverification tools Providing detailed examinations contributed by leading experts Low Power Processors and Systems on Chips supplies authoritative information on how to maintain high performance while lowering power consumption in modern processors and SoCs It is a must read for anyone designing modern computers or embedded systems

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Low Power Design With High Level Power Estimation And Power Aware Synthesis Introduction

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