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High Dielectric Constant Materials

VLSI MOSFET
Applications



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High Dielectric Constant Materials Vlsi Mosfet Applications Springer Series In Advanced Microelectronics

Friedel Gerfers, Maurits Ortmanns



High Dielectric Constant Materials Vlsi Mosfet Applications Springer Series In Advanced Microelectronics:

High Dielectric Constant Materials Howard Huff, 2005 Issues relating to the high K gate dielectric are among the greatest challenges for the evolving International Technology Roadmap for Semiconductors ITRS More than just an historical overview this book will assess previous and present approaches related to scaling the gate dielectric and their impact along with the creative directions and forthcoming challenges that will define the future of gate dielectric scaling technology Topics include an extensive review of Moore's Law the classical regime for SiO₂ gate dielectrics the transition to silicon oxynitride gate dielectrics the transition to high K gate dielectrics including the drive towards equivalent oxide thickness in the single digit nanometer regime and future directions and issues for ultimate technology generation scaling The vision wisdom and experience of the team of authors will make this book a timely relevant and interesting resource focusing on fundamentals of the 45 nm Technology Generation and beyond *Reliability of high-k / metal gate field-effect transistors considering circuit operational constraints* Steve Kupke, 2016-06-06 After many decades the scaling of silicon dioxide based field effect transistors has reached insurmountable physical limits due to unintentional high gate leakage currents for gate oxide thicknesses below 2 nm The introduction of high k metal gate stacks guaranteed the trend towards smaller transistor dimensions The implementation of HfO₂ as high k dielectric also led to a substantial number of manufacturing and reliability challenges The deterioration of the gate oxide properties under thermal and electric stress jeopardizes the circuit operation and hence needs to be comprehensively understood As a starting point 6T static random access memory cells were used to identify the different single device operating conditions The strongest deterioration of the gate stack was found for nMOS devices under positive bias temperature instability (PBTI) stress resulting in a severe threshold voltage shift and increased gate leakage current A detailed investigation of physical origin and temperature and voltage dependency was done The reliability issues were caused by the electron trapping into already existing HfO₂ oxygen vacancies The oxygen vacancies reside in different charge states depending on applied stress voltages This in return also resulted in a strong threshold voltage and gate current relaxation after stress was cut off The reliability assessment using constant voltage stress does not reflect realistic circuit operation which can result in a changed degradation behaviour Therefore the constant voltage stress measurements were extended by considering CMOS operational constraints where it was found that the supply voltage frequently switches between the gate and drain terminal The additional drain off state bias led to an increased V_t relaxation in comparison to zero bias voltage The off state influence strongly depended on the gate length and became significant for short channel devices The influence of the off state bias on the dielectric breakdown was studied and compared to the standard assessment methods Different wear out mechanisms for drain only and alternating gate and drain stress were verified Under drain only stress the dielectric breakdown was caused by hot carrier degradation The lifetime was correlated with the device length and amount of subthreshold leakage The gate oxide breakdown under alternating gate and

o state stress was caused by the continuous trapping and detrapping behaviour of high k metal gate devices

Characterization of Semiconductor Heterostructures and Nanostructures Andre Stesmans, Valery V.

Afanas'ev, 2013-04-11 **System-level Test and Validation of Hardware/Software Systems** Matteo Sonza Reorda, Zebo Peng, Massimo Violante, 2006-03-30 New manufacturing technologies have made possible the integration of entire systems on a single chip This new design paradigm termed system on chip SOC together with its associated manufacturing problems represents a real challenge for designers SOC is also reshaping approaches to test and validation activities These are beginning to migrate from the traditional register transfer or gate levels of abstraction to the system level Until now test and validation have not been supported by system level design tools so designers have lacked the infrastructure to exploit all the benefits stemming from the adoption of the system level of abstraction Research efforts are already addressing this issue This monograph provides a state of the art overview of the current validation and test techniques by covering all aspects of the subject including modeling of bugs and defects stimulus generation for validation and test purposes including timing errors design for testability **Silicon Nitride, Silicon Dioxide, and Emerging Dielectrics 9** R. Ekwil Sah, 2007 This issue of ECS Transactions contains the papers presented in the symposium on Silicon Nitride Silicon Dioxide Thin Insulating Films and Emerging Dielectrics held May 6 11 2007 in Chicago Papers were presented on deposition characterization and applications of the dielectrics including high and low k dielectrics as well as interface states device characterization reliability and modeling Timing Performance of Nanometer Digital Circuits Under Process Variations Victor Champac, Jose Garcia Gervacio, 2018-04-18 This book discusses the digital design of integrated circuits under process variations with a focus on design time solutions The authors describe a step by step methodology going from logic gates to logic paths to the circuit level Topics are presented in comprehensively without overwhelming use of analytical formulations Emphasis is placed on providing digital designers with understanding of the sources of process variations their impact on circuit performance and tools for improving their designs to comply with product specifications Various circuit level design hints are highlighted so that readers can use them to improve their designs A special treatment is devoted to unique design issues and the impact of process variations on the performance of FinFET based circuits This book enables readers to make optimal decisions at design time toward more efficient circuits with better yield and higher reliability **Defects in High-k Gate Dielectric Stacks** Evgeni Gusev, 2006-01-27 The main goal of this book is to review at the nano and atomic scale the very complex scientific issues that pertain to the use of advanced high dielectric constant high k materials in next generation semiconductor devices One of the key obstacles to integrate this novel class of materials into Si nano technology are the electronic defects in high k dielectrics It has been established that defects do exist in high k dielectrics and they play an important role in device operation The unique feature of this book is a special focus on the important issue of defects The subject is covered from various angles including silicon technology processing aspects materials properties electrical defects

microstructural studies and theory The authors who have contributed to the book represents a diverse group of leading scientists from academic industrial and governmental labs worldwide who bring a broad array of backgrounds basic and applied physics chemistry electrical engineering surface science and materials science The contributions to this book are accessible to both expert scientists and engineers who need to keep up with leading edge research and newcomers to the field who wish to learn more about the exciting basic and applied research issues relevant to next generation device technology Microcontrollers in Practice Ioan Susnea,Marian Mitescu,2005-07-06 Stressing common characteristics and real applications of the most used microcontrollers this practical guide provides readers with hands on knowledge of how to implement three families of microcontrollers HC11 AVR and 8051 Unlike the rest of the ocean of literature on individual chips Microcontrollers in Practice supplies side by side comparisons and an overview that treats the systems as resources available for implementation Packed with hundreds of practical examples and exercises to foster mastery of concepts and details the guide also includes several extended projects By treating the less expensive 8 bit and RISC microcontrollers this information dense manual equips students and home experimenters with the know how to put these devices into operation

Power Management of Digital Circuits in Deep Sub-Micron CMOS Technologies Stephan Henzler,2006-11-24 In the deep sub micron regime the power consumption has become one of the most important issues for competitive design of digital circuits Due to dramatically increasing leakage currents the power consumption does not take advantage of technology scaling as before State of art power reduction techniques like the use of multiple supply and threshold voltages transistor stack forcing and power gating are discussed with respect to implementation and power saving capability Focus is given especially on technology dependencies process variations and technology scaling Design and implementation issues are discussed with respect to the trade off between power reduction performance degradation and system level constraints A complete top down design flow is demonstrated for power gating techniques introducing new design methodologies for the switch sizing task and circuit blocks for data retention and block activation The leakage reduction ratio and the minimum power down time are introduced as figures of merit to describe the power gating technique on system level and give a relation to physical circuit parameters Power Management of Digital Circuits in Deep Sub Micron CMOS Technologies mainly deals with circuit design but also addresses the interface between circuit and system level design on the one side and between circuit and physical design on the other side **Gettering Defects in Semiconductors** Victor A.

Perevostchikov,Vladimir D. Skoupov,2005-09-15 Gettering Defects in Semiconductors fulfills three basic purposes to systematize the experience and research in exploiting various gettering techniques in microelectronics and nanoelectronics to identify new directions in research particularly to enhance the perspective of professionals and young researchers and specialists to fill a gap in the contemporary literature on the underlying semiconductor material theory The authors address not only well established gettering techniques but also describe contemporary trends in gettering technologies from an

international perspective The types and properties of structural defects in semiconductors their generating and their transforming mechanisms during fabrication are described The primary emphasis is placed on classifying and describing specific gettering techniques their specificity arising from both their position in a general technological process and the regimes of their application This book addresses both engineers and material scientists interested in semiconducting materials theory and also undergraduate and graduate students in solid state microelectronics and nanoelectronics A comprehensive list of references provides readers with direction for further reading

Characterization of Semiconductor Heterostructures and Nanostructures Giovanni Agostini, Carlo Lamberti, 2013-04-11

Characterization of Semiconductor Heterostructures and Nanostructures is structured so that each chapter is devoted to a specific characterization technique used in the understanding of the properties structural physical chemical electrical etc of semiconductor quantum wells and superlattices An additional chapter is devoted to ab initio modeling The book has two basic aims The first is educational providing the basic concepts of each of the selected techniques with an approach understandable by advanced students in Physics Chemistry Material Science Engineering Nanotechnology The second aim is to provide a selected set of examples from the recent literature of the TOP results obtained with the specific technique in understanding the properties of semiconductor heterostructures and nanostructures Each chapter has this double structure the first part devoted to explain the basic concepts and the second to the discussion of the most peculiar and innovative examples The topic of quantum wells wires and dots should be seen as a pretext of applying top level characterization techniques in understanding the structural electronic etc properties of matter at the nanometer and even sub nanometer scale In this respect it is an essential reference in the much broader and extremely hot field of Nanotechnology Comprehensive collection of the most powerful characterization techniques for semiconductors heterostructures and nanostructures Most of the chapters are authored by scientists that are world wide among the top ten in publication ranking of the specific field Each chapter starts with a didactic introduction on the technique The second part of each chapters deals with a selection of top examples highlighting the power of the specific technique to analyse the properties of semiconductors heterostructures and nanostructures

High-Dynamic-Range (HDR) Vision Bernd Hoefflinger, 2007-02-16

Creating high fidelity images of our world has been a continuous challenge even as our understanding and skills have evolved The acquisition and mapping of the rich and complex content of visual information rank high among the most demanding technical tasks Now electronic image sensors can record a dynamic range from bright to dark of more than seven orders of magnitude thus exceeding the ability of a human eye by more than a hundred times and displaying five orders of magnitude in brightness resulting in CRT and LCD displays with more than 100 fold improvement This first comprehensive account of high dynamic range HDR vision focusses on HDR real time high speed digital video recording and also systematically presents HDR video transmission and display The power of the eye like logarithmic optoelectronic conversion concept is demonstrated in machine vision medical

automotive surveillance and cinematic applications and it is extended to HDR sub retinal implants for the vision impaired While the book conveys the overall picture of HDR vision specific knowledge of microelectronics and image processing is not required It provides a quantitative summary of the major issues to allow the assessment of the state of the art and a glimpse at future developments Selected experts share their know how and expectations in this rapidly evolving art related to the single most powerful of our senses

Highly Sensitive Optical Receivers Kerstin Schneider,2006-11-10 Highly Sensitive Optical Receivers primarily treats the circuit design of optical receivers with external photodiodes Continuous mode and burst mode receivers are compared The monograph first summarizes the basics of III V photodetectors transistor and noise models bit error rate sensitivity and analog circuit design thus enabling readers to understand the circuits described in the main part of the book In order to cover the topic comprehensively detailed descriptions of receivers for optical data communication in general and in particular optical burst mode receivers in deep sub m CMOS are presented Numerous detailed and elaborate illustrations facilitate better understanding

Detection and Signal Processing Wilhelmus Jacobus Witteman,2007-04-14 This comprehensive monograph deals with detectors signal processors and related noise phenomena Detailed quantitative analyses are developed in a consistent format for thermal detectors vacuum detectors semiconductor detectors and avalanche detectors as well as their accompanying noise currents For signal processing applications the monograph treats in detail the operational amplifier signal averagers waveform analyzers correlation techniques and heterodyne detection Several original extensions are reported especially for correlation devices and heterodyne detection with noise rejection In addition results of analyses are illustrated with examples of operating systems and of applications in space communication and laser radar

Characterization of Semiconductor Heterostructures and Nanostructures Carlo Lamberti,2008-08-19 Comprehensive collection of the most powerful characterization techniques for semiconductors heterostructures and nanostructures Most of the chapters are authored by scientists that are world wide among the top ten in publication ranking of the specific field Each chapter starts with a didactic introduction on the technique The second part of each chapters deals with a selection of top examples highlighting the power of the specific technique to analyse the properties of semiconductors heterostructures and nanostructures

Extending Moore's Law through Advanced Semiconductor Design and Processing Techniques Wynand Lambrechts,Saurabh Sinha,Jassem Ahmed Abdallah,Jaco Prinsloo,2018-09-13 This book provides a methodological understanding of the theoretical and technical limitations to the longevity of Moore s law The book presents research on factors that have significant impact on the future of Moore s law and those factors believed to sustain the trend of the last five decades Research findings show that boundaries of Moore s law primarily include physical restrictions of scaling electronic components to levels beyond that of ordinary manufacturing principles and approaching the bounds of physics The research presented in this book provides essential background and knowledge to grasp the following principles Traditional and modern photolithography the primary limiting factor of Moore s

law Innovations in semiconductor manufacturing that makes current generation CMOS processing possible Multi disciplinary technologies that could drive Moore s law forward significantly Design principles for microelectronic circuits and components that take advantage of technology miniaturization The semiconductor industry economic market trends and technical driving factors The complexity and cost associated with technology scaling have compelled researchers in the disciplines of engineering and physics to optimize previous generation nodes to improve system on chip performance This is especially relevant to participate in the increased attractiveness of the Internet of Things IoT This book additionally provides scholarly and practical examples of principles in microelectronic circuit design and layout to mitigate technology limits of previous generation nodes Readers are encouraged to intellectually apply the knowledge derived from this book to further research and innovation in prolonging Moore s law and associated principles

High-k Gate Dielectric Materials Niladri Pratap Maity, Reshmi Maity, Srimanta Baishya, 2020-12-18 This volume explores and addresses the challenges of high k gate dielectric materials one of the major concerns in the evolving semiconductor industry and the International Technology Roadmap for Semiconductors ITRS The application of high k gate dielectric materials is a promising strategy that allows further miniaturization of microelectronic components This book presents a broad review of SiO₂ materials including a brief historical note of Moore s law followed by reliability issues of the SiO₂ based MOS transistor It goes on to discuss the transition of gate dielectrics with an EOT 1 nm and a selection of high k materials A review of the various deposition techniques of different high k films is also discussed High k dielectrics theories quantum tunneling effects and interface engineering theory and applications of different novel MOSFET structures like tunneling FET are also covered in this book The volume also looks at the important issues in the future of CMOS technology and presents an analysis of interface charge densities with the high k material tantalum pentoxide The issue of CMOS VLSI technology with the high k gate dielectric materials is covered as is the advanced MOSFET structure with its working structure and modeling This timely volume will prove to be a valuable resource on both the fundamentals and the successful integration of high k dielectric materials in future IC technology

Continuous-Time Sigma-Delta A/D Conversion Friedel Gerfers, Maurits Ortmanns, 2006-02-27 Sigma delta A D converters are a key building block in wireless and multimedia applications This comprehensive book deals with all relevant aspects arising during the analysis design and simulation of the now widespread continuous time implementations of sigma delta modulators The results of several years of research by the authors in the field of CT sigma delta modulators are covered including the analysis and modeling of different CT modulator architectures CT DT loop filter synthesis a detailed error analysis of all components and possible compensation correction schemes for the non ideal behavior in CT sigma delta modulators Guidance for obtaining low power consumption and several practical implementations are also presented It is shown that all the proposed new theories architectures and possible correction techniques have been confirmed by measurements on discrete or integrated circuits Quantitative results are also provided thus enabling prediction of the

resulting accuracy Implantable Neural Prostheses 2 David Zhou, Elias Greenbaum, 2010-07-10 Significant progress has been made in the development of neural prostheses for restoration of human functions and improvement of the quality of life. Biomedical engineers and neuroscientists around the world are working to improve the design and performance of existing devices and to develop novel devices for artificial vision, artificial limbs and brain-machine interfaces. This book, Implantable Neural Prostheses 2: Techniques and Engineering Approaches, is part two of a two-volume sequence that describes state-of-the-art advances in techniques associated with implantable neural prosthetic devices. The techniques covered include biocompatibility and biostability, hermetic packaging, electrochemical techniques for neural stimulation applications, novel electrode materials and testing, thin-film-exible microelectrode arrays, in situ characterization of microelectrode arrays, chip-size thin-film device encapsulation, microchip embedded capacitors and microelectronics for recording, stimulation and wireless telemetry. The design process in the development of medical devices is also discussed. Advances in biomedical engineering, microfabrication technology and neuroscience have led to improved medical device designs and novel functions. However, many challenges remain. This book focuses on the engineering approaches, R D advances and technical challenges of medical implants from an engineering perspective. We are grateful to leading researchers from academic institutes, national laboratories as well as design engineers and professionals from the medical device industry who have contributed to the book. Part one of this series covers designs of implantable neural prosthetic devices and their clinical applications. The British National Bibliography Arthur James Wells, 2004

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