

Transactions on **High-Performance Embedded Architectures and Compilers IV**

Per Stenström
Editor-in-Chief



High Performance Embedded Architectures And Compilers High Performance Embedded Architectures And Compilers

Sid Touati, Benoit Dupont de Dinechin

High Performance Embedded Architectures And Compilers High Performance Embedded Architectures And Compilers:

High Performance Embedded Architectures and Compilers Tom Conte, Nacho Navarro, Wen-mei W. Hwu, Mateo Valero, Theo Ungerer, 2005-10-27 As Chairmen of HiPEAC 2005 we have the pleasure of welcoming you to the proceedings of the first international conference promoted by the HiPEAC Network of Excellence During the last year HiPEAC has been building its clusters of researchers in computer architecture and advanced compiler techniques for embedded and high performance computers Recently the Summer School has been the seed for a fruitful collaboration of renowned international faculty and young researchers from 23 countries with fresh new ideas Now the conference promises to be among the premier forums for discussion and debate on these research topics The prestige of a symposium is mainly determined by the quality of its technical program This first program lived up to our high expectations thanks to the large number of strong submissions The Program Committee received a total of 84 submissions only 17 were selected for presentation as full length papers and another one as an invited paper Each paper was rigorously reviewed by three Program Committee members and at least one external referee Many reviewers spent a great amount of effort to provide detailed feedback In many cases such feedback along with constructive shepherding resulted in dramatic improvement in the quality of accepted papers The names of the Program Committee members and the referees are listed in the proceedings The net result of this team effort is that the symposium proceedings include outstanding contributions by authors from nine countries in three continents In addition to paper presentations this first HiPEAC conference featured two keynotes delivered by prominent researchers from industry and academia

High Performance Embedded Architectures and Compilers Koen De Bosschere, David Kaeli, Per Stenström, David Whalley, Theo Ungerer, 2007-07-20 This book constitutes the refereed proceedings of the Second International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2007 held in Ghent Belgium in January 2007 The 19 revised full papers presented together with one invited keynote paper were carefully reviewed and selected from 65 submissions The papers are organized in topical sections

Transactions on High-Performance Embedded Architectures and Compilers V Cristina Silvano, Koen Bertels, Michael Schulte, 2019-02-22 Transactions on HiPEAC aims at the timely dissemination of research contributions in computer architecture and compilation methods for high performance embedded computer systems Recognizing the convergence of embedded and general purpose computer systems this journal publishes original research on systems targeted at specific computing tasks as well as systems with broad application bases The scope of the journal therefore covers all aspects of computer architecture code generation and compiler optimization methods of interest to researchers and practitioners designing future embedded systems This 5th issue contains extended versions of papers by the best paper award candidates of IC SAMOS 2009 and the SAMOS 2009 Workshop colocated events of the 9th International Symposium on Systems Architectures Modeling and Simulation SAMOS 2009 held

in Samos Greece in 2009 The 7 papers included in this volume were carefully reviewed and selected The papers cover research on embedded processor hardware software design and integration and present challenging research trends

High Performance Embedded Architectures and Compilers Yale N. Patt,Pierfrancesco Foglia,Evelyn Duesterwald,Paolo Faraboschi,Xavier Martorell,2010-01-20 This book constitutes the refereed proceedings of the 5th International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2010 held in Pisa Italy in January 2010 The 23 revised full papers presented together with the abstracts of 2 invited keynote addresses were carefully reviewed and selected from 94 submissions The papers are organized in topical sections on architectural support for concurrency compilation and runtime systems reconfigurable and customized architectures multicore efficiency reliability and power memory organization and optimization and programming and analysis of accelerators

Transactions on High-Performance Embedded Architectures and Compilers I Mike O'Boyle,Francois Bodin,Marcelo Cintra,Sally A. McKee,2007-07-21 Transactions on HiPEAC is a new journal which aims at the timely dissemination of research contributions in computer architecture and compilation methods for high performance embedded computer systems It publishes original research on systems targeted at specific computing tasks as well as systems with broad application bases Its scope covers all aspects of computer architecture code generation and compiler optimization methods

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IEEE International Symposium on Systems Architectures Modeling and Simulation SAMOS VIII 2008 held in Samos Greece in July 2008 Transactions on High-performance Embedded Architectures and Compilers V Per Stenström, 2019 Transactions on HiPEAC aims at the timely dissemination of research contributions in computer architecture and compilation methods for high performance embedded computer systems Recognizing the convergence of embedded and general purpose computer systems this journal publishes original research on systems targeted at specific computing tasks as well as systems with broad application bases The scope of the journal therefore covers all aspects of computer architecture code generation and compiler optimization methods of interest to researchers and practitioners designing future embedded systems This 5th issue contains extended versions of papers by the best paper award candidates of IC SAMOS 2009 and the SAMOS 2009 Workshop colocated events of the 9th International Symposium on Systems Architectures Modeling and Simulation SAMOS 2009 held in Samos Greece in 2009 The 7 papers included in this volume were carefully reviewed and selected The papers cover research on embedded processor hardware software design and integration and present challenging research trends

High Performance Embedded Architectures and Compilers André Seznec, Michael O'Boyle, Joel Emer, Margaret Martonosi, Theo Ungerer, 2009-01-12 This book constitutes the refereed proceedings of the Fourth International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2009 held in Paphos Cyprus in January 2009 The 27 revised full papers presented together with 2 invited keynote paper were carefully reviewed and selected from 97 submissions The papers are organized in topical sections on dynamic translation and optimisation low level scheduling parallelism and resource control communication mapping for CMPs power cache issues as well as parallel embedded applications **High Performance Embedded Architectures and Compilers** Per Stenström, Michel Dubois, Manolis Katevenis, Rajiv Gupta, Theo Ungerer, 2008-01-15 This highly relevant and up to the minute book constitutes the refereed proceedings of the Third International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2008 held in Göteborg Sweden January 27 29 2008 The 25 revised full papers presented together with 1 invited keynote paper were carefully reviewed and selected from 77 submissions The papers are organized into topical sections on a number of key subjects in the field *Transactions on High-Performance Embedded Architectures and Compilers II* Per

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the 2nd International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2007 held in Ghent Belgium in January 2007 The second section consists of ten papers covering topics such as microarchitecture memory systems code generation and performance modeling Transactions on High-Performance Embedded Architectures and Compilers III Per Stenström, 2011-04-28 Transactions on HiPEAC aims at the timely dissemination of research contributions in computer architecture and compilation methods for high performance embedded computer systems Recognizing the convergence of embedded and general purpose computer systems this journal publishes original research on systems targeted at specific computing tasks as well as systems with broad application bases The scope of the journal therefore covers all aspects of computer architecture code generation and compiler optimization methods of interest to researchers and practitioners designing future embedded systems This third issue contains 14 papers carefully reviewed and selected out of numerous submissions and is divided into four sections The first section contains the top four papers from the Third International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2008 held in Göteborg Sweden in January 2008 The second section consists of four papers from the 8th MEDEA Workshop held in conjunction with PACT 2007 in Brasov Romania in September 2007 The third section contains two regular papers and the fourth section provides a snapshot from the First Workshop on Programmability Issues for Multicore Computers MULTIPROG held in conjunction with HiPEAC 2008 *Transactions on High-Performance Embedded Architectures and Compilers II* Per Stenström, David Whalley, 2009-04-22 This book contains extended versions of key papers from the 2nd International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2007 It also covers such topics as microarchitecture code generation and performance modeling High-Performance Embedded Computing Wayne Wolf, 2010-07-26 Over the past several years embedded systems have emerged as an integral though unseen part of many consumer industrial and military devices The explosive growth of these systems has resulted in embedded computing becoming an increasingly important discipline The need for designers of high performance application specific computing systems has never been greater and many universities and colleges in the US and worldwide are now developing advanced courses to help prepare their students for careers in embedded computing High Performance Embedded Computing Architectures Applications and Methodologies is the first book designed to address the needs of advanced students and industry professionals Focusing on the unique complexities of embedded system design the book provides a detailed look at advanced topics in the field including multiprocessors VLIW and superscalar architectures and power consumption Fundamental challenges in embedded computing are described together with design methodologies and models of computation HPEC provides an in depth and advanced treatment of all the components of embedded systems with discussions of the current developments in the field and numerous examples of real world applications Covers advanced topics in embedded computing including multiprocessors VLIW and superscalar architectures and power consumption

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color This new edition of the handbook is organized in three parts Part I motivates representative applications that drive and apply state of the art methods for design and implementation of signal processing systems Part II discusses architectures for implementing these applications and Part III focuses on compilers as well as models of computation and their associated design tools and methodologies

Model-Implementation Fidelity in Cyber Physical System Design Anca Molnos,Christian Fabre,2016-12-08 This book puts in focus various techniques for checking modeling fidelity of Cyber Physical Systems CPS with respect to the physical world they represent The authors present modeling and analysis techniques representing different communities from very different angles discuss their possible interactions and discuss the commonalities and differences between their practices Coverage includes model driven development resource driven development statistical analysis proofs of simulator implementation compiler construction power temperature modeling of digital devices high level performance analysis and code device certification Several industrial contexts are covered including modeling of computing and communication proof architectures models and statistical based validation techniques

Advanced Backend Code Optimization Sid Touati,Benoit Dupont de Dinechin,2014-06-02 This book is a summary of more than a decade of research in the area of backend optimization It contains the latest fundamental research results in this field While existing books are often more oriented toward Masters students this book is aimed more towards professors and researchers as it contains more advanced subjects It is unique in the sense that it contains information that has not previously been covered by other books in the field with chapters on phase ordering in optimizing compilation register saturation in instruction level parallelism code size reduction for software pipelining memory hierarchy effects and instruction level parallelism Other chapters provide the latest research results in well known topics such as register need and software pipelining and periodic register allocation

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