High-Performance Energy-Efficient Microprocessor Design

Edited by

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2 Springer

Hubert Kaeslin

High-Performance Energy-Efficient Microprocessor Design Vojin G. Oklobdzija, Ram K. Krishnamurthy, 2007-04-27 Microprocessors of today contain close to a billion transistors while achieving the performance of super computers just a decade ago Designing such processors takes hundreds of people organized into large teams High Performance Energy Efficient Microprocessor Design is written by the world's most prominent microprocessor design leaders from the industry and academia It provides a complete coverage of all the aspects of a complex microprocessor design process from technology power management clocking high performance architecture design methodologies memory and I O design computer aided design testing and design for testability The chapters are written to provide the latest state of the art knowledge of particular aspects of microprocessor design while including sufficient tutorial content in order to bring non experts up to speed High Performance Energy Efficient Microprocessor Design is intended to be a useful companion book for every design engineer working in the related areas and a source of technical information as well as a comprehensive reference in the field It should also serve as the source book for technical and business managers involved in microprocessor based design and manufacture The chapters are organized in a way which makes it possible to use this book as a textbook for graduate courses in advanced digital and system design The book is intended to highlight practical problems encountered in designing state of the art processors while yet covering fundamental principles that are independent of technology **Energy Efficient** Microprocessor Design Thomas D. Burd, Robert W. Brodersen, 2012-12-06 This work began in 1995 as an outgrowth of the InfoPad project which showed us that in order to reduce the energy consumption of a portable multimedia terminal that something had to be done about the consumption of the microprocessor subsystem. The design of the InfoPad attempted to reduce the requirements of this general pur pose processor by moving the computation into the network or by the use of highly optimized integrated circuits but in spite of these efforts it still was a major consumer of energy. The reasons for this became apparent as we determined that the energy required to perform a function in dedicated hardware could be several orders of magnitude lower than that consumed in the InfoPad microprocessor We therefore set out on a full fledged attack on all aspects of the microprocessor energy consumption 1 J After considerable analysis it became clear that though better circuit design and a stream lined architecture would assist in our goal of energy reduction that the biggest gains were to be found by operating at reduced voltages For the busses and VO this could be accomplished without significant degradation of the processor performance but this was not a straightforward solution when applied to the core of the processor sub system CPU and memory High-Performance Energy-Efficient Microprocessor Design Vojin G. Oklobdzija, Ram K. Krishnamurthy, 2008-11-01 Written by the world's most prominent microprocessor design leaders from industry and academia this book provides complete coverage of all aspects of complex microprocessor design technology power management clocking high performance architecture design methodologies memory and I O design computer aided design

testing and design for testability The chapters provide state of the art knowledge while including sufficient tutorial material to bring non experts up to speed A useful companion to design engineers working in related areas — Digital Integrated Circuit Design Hubert Kaeslin, 2008-04-28 This practical tool independent guide to designing digital circuits takes a unique top down approach reflecting the nature of the design process in industry Starting with architecture design the book comprehensively explains the why and how of digital circuit design using the physics designers need to know and no more

Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation José L. Ayala, Delong Shang, Alex Yakovley, 2013-01-03 This book constitutes the refereed proceedings of the 22nd International Conference on Integrated Circuit and System Design PATMOS 2012 held in Newcastle UK Spain in September 2012 The 25 revised full papers presented were carefully reviewed and selected from numerous submissions. The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems including reconfigurable hardware such as FPGAs The technical program focus on timing performance and power consumption as well as architectural aspects with particular emphasis on modeling design characterization analysis and optimization **Practical Introduction to PSL** Cindy Eisner, Dana Fisman, 2007-06-19 Functional veri cation is hard Period No disagreement here But why is this so Consider today s design ow much of it is more or less automated from RTL to netlist to layout to silicon But all this automation depends upon having correct RTL input to start with and there is little or no automation to help with RTL creation It is hard enough for a designer to decide what RTL model he wants to build and then to describe that RTL model correctly in a hardware description language It is even more di cult for a veri cation engineer who can t read the designer's mind to verify that what the designer created not only represents the RTL model he had conceived but also that the RTL model is an appropriate one for the problem at hand What makes RTL modeling and veri cation di cult is concurrency It is easy to teach an engineer how to write procedural code that conforms to the synthesizable subset of a hardware description language What is hard is understanding how the engineer's procedural code interacts with other c ponents in the design over time In fact until recently we lacked e ective languages to describe concurrent behaviors The IEEE 1850 Property Speci cation Language PSL is a language for the formal speci cation of concurrent systems The language is particularly applicable for writing assertions about hardware designs PSL supports m tiple veri cation paradigms including formal analysis simulation and acc eration emulation Advanced Circuits for Emerging Technologies Krzysztof Iniewski, 2012-04-17 The book will address the state of the art in integrated circuit design in the context of emerging systems New exciting opportunities in body area networks wireless communications data networking and optical imaging are discussed Emerging materials that can take system performance beyond standard CMOS like Silicon on Insulator SOI Silicon Germanium SiGe and Indium Phosphide InP are explored Three dimensional 3 D CMOS integration and co integration with sensor technology are described as well The book is a must for anyone serious about circuit design for

future technologies. The book is written by top notch international experts in industry and academia. The intended audience is practicing engineers with integrated circuit background The book will be also used as a recommended reading and supplementary material in graduate course curriculum Intended audience is professionals working in the integrated circuit design field Their job titles might be design engineer product manager marketing manager design team leader etc The book will be also used by graduate students Many of the chapter authors are University Professors Integrated Circuit and System Design: Power and Timing Modeling, Optimization and Simulation José Monteiro, Rene van Leuken, 2010-02-18 This book constitutes the thoroughly referred post conference proceedings of 19th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2009 featuring Integrated Circuit and System Design held in Delft The Netherlands during September 9 11 2009 The 26 revised full papers and 10 revised poster papers presented were carefully reviewed and selected from numerous submissions The papers are organized in topical sections on variability statistical timing circuit level techniques power management low power circuits technology system level techniques power timing optimization techniques self timed circuits low power circuit analysis optimization and low power design studies **3D Integration for VLSI Systems** Chuan Seng Tan, 2011 Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation Jorge Juan Chico, Enrico Macii, 2003-09-03 This book constitutes the refereed proceedings of the 13th International Workshop on Power and Timing Modeling Optimization and Simulation PATMOS 2003 held in Torino Italy in September 2003 The 43 revised full papers and 18 revised poster papers presented together with three keynote contributions were carefully reviewed and selected from 85 submissions. The papers are organized in topical sections on gate level modeling and characterization interconnect modeling and optimization asynchronous techniques RTL power modeling and memory optimization high level modeling power efficient technologies and designs communication modeling and design and low power issues in processors and multimedia **High-Performance System Design** Vojin G. Oklobdzija, 1999-07-12 This comprehensive collection of papers offers you practical information that can be used to develop high performance digital system design Specially written introductions by editor Vojin G Oklobdzija precede each chapter to aid your understanding of the most relevant topics in this advanced area of circuit design Featured topics include Differential pass transistor logic High speed circuits and design of high performance systems Advanced deep submicron circuits used in high speed computers and digital circuits Clocking and latch design essential to high performance systems Relationships between VLSI algorithms and implementation techniques HIGH PERFORMANCE SYSTEM DESIGN Circuits and Logic is indispensable reading for circuit designers practicing engineers and students who want to master the basic principles underlying high performance system design This handy single volume provides a useful reference to a collection of accumulated experience necessary for good successful designs Professors To request an examination copy simply e mail collegeadoption ieee org Sponsored by IEEE Solid State Circuits Council Society Sub-threshold Design for Ultra

Low-Power Systems Alice Wang, Benton Highsmith Calhoun, Anantha P. Chandrakasan, 2006-12-11 Based on the work of MIT graduate students Alice Wang and Benton Calhoun this book surveys the field of sub threshold and low voltage design and explores such aspects of sub threshold circuit design as modeling logic and memory circuit design One important chapter of the book is dedicated to optimizing energy dissipation a key metric for energy constrained designs This book also includes invited chapters on the subject of analog sub threshold circuits *Introduction to Low-Power Design in VLSIs* Patrick Lee, 2011-12-12 This book discusses one increasingly important issue in the VLSI design low power It covers the following topics a basic concepts of low power design b low power design methods and applications in industry chips and c commercial CAD tools on low power design This book discusses the concepts a set of known methods industry cases and CAD tools on the low power design It is organized in four chapters and a glossary is provided at the end of the book Third International Conference on Information Management and Machine Intelligence Dinesh Goyal, Anil Kumar, Vincenzo Piuri, Marcin Paprzycki, 2022-08-03 This book features selected papers presented at Third International Conference on International Conference on Information Management and Machine Intelligence ICIMMI 2021 held at Poornima Institute of Engineering AI machine and deep learning information management security processing techniques and interpretation applications of artificial intelligence in soft computing and pattern recognition cloud based applications for machine learning application of IoT in power distribution systems as well as wireless sensor networks and adaptive wireless Ultra-Low Voltage Nano-Scale Memories Kiyoo Itoh, Masashi Horiguchi, Hitoshi Tanaka, 2007-09-04 Ultra communication Low Voltage Nano Scale Memories provides an in depth discussion of the state of the art nanometer and sub 1 V memory LSIs that are playing decisive roles in power conscious systems Emerging problems between the device circuit and system levels are systematically covered in terms of reliable high speed operations of memory cells and peripheral logic circuits The effectiveness of solutions at device and circuit levels is also described at length through clarifying noise components in an array and even essential differences in ultra low voltage operations between DRAMs and SRAMs Moreover various kinds of on chip voltage converters necessary to solve problems with internal power supply managements are extensively discussed This authoritative monograph addresses these design challenges for memory and circuit engineers as well as for researchers and students who are interested in ultra low voltage nano scale memory LSIs **Abstraction Refinement for Large Scale** Model Checking Chao Wang, Gary D. Hachtel, Fabio Somenzi, 2006-09-15 Abstraction Refinement for Large Scale Model Checking summarizes recent research on abstraction techniques for model checking large digital system Considering both the size of today s digital systems and the capacity of state of the art verification algorithms abstraction is the only viable solution for the successful application of model checking techniques to industrial scale designs This book describes recent research developments in automatic abstraction refinement techniques. The suite of algorithms presented in this book has demonstrated significant improvement over prior art some of them have already been adopted by the EDA companies in their

commercial in house verification tools Integrated Circuit and System Design. Power and Timing Modeling, Optimization, and Simulation Rene van Leuken, Gilles Sicard, 2011-02-04 This book constitutes the refereed proceedings of the 20th International Conference on Integrated Circuit and System Design PATMOS 2010 held in Grenoble France in September 2010 The 24 revised full papers presented and the 9 extended abstracts were carefully reviewed and are organized in topical sections on design flows circuit techniques low power circuits self timed circuits process variation high level modeling of poweraware heterogeneous designs in SystemC AMS and minalogic **Ultra-Low Power Wireless Technologies for** Sensor Networks Brian Otis, Jan Rabaey, 2007-02-24 transconductance e ciency of all critical devices in order to reduce the n essary bias current However reducing the current density also results in a severely decreased device f An optimization of the current density is re T quired to provide the correct balance between transconductance e ciency and bandwidth Plots such as Figure 2.1 are useful tools for designers when choosing appropriate transistor bias points Technology scaling allows greatly increased f realization for a given IC Thus weak inversion biasing for RF T design will become increasingly useful in future technology nodes Throughout this work the IC of critical transistors will be discussed Most of the RF devices are biased in moderate to weak inversion to achieve enhanced transconductance e ciency and reduced bias current 2 2 MEMS Background The relatively new eld of Radio Frequency Microelectro Mechanical Systems RF MEMS provides unique opportunities for RF transceiver designers This section provides background on RF MEMS and provides insight into the portunities presented by these new technologies The eld of RF MEMS cludes the design and utilization of RF lters resonators switches and other passive mechanical structures constructed using bulk processed integrated c cuit fabrication techniques To date these devices have been commercially used as discrete board mounted components primarily used to enhance the miniaturization of mobile phones However RF MEMS components have the potential to be batch fabricated using existing integrated circuit fabrication techniques Leveraging AI for Innovative Sustainable Energy: Solar, Wind and Green **Hydrogen** Hammouch, Hind, Razzak Janjua, Laeeg, 2025-05-15 Artificial intelligence AI and intelligent technologies play a vital role in transforming the energy sector which is key to delivering lower carbon footprints combined with increased levels of security AI driven innovations in solar wind energy green hydrogen generation increase efficiency to achieve further sustainability Furthermore the disruptive impact of AI based solutions in the energy sector is informative for initiating more sustainable industrial and commercial purposes and practices worldwide Thus AI enabled systems and their capabilities in generation distribution of energy and consumption can contribute to helping build more robust and greener infrastructures for our resources Leveraging AI for Innovative Sustainable Energy Solar Wind and Green Hydrogen offers practical steps for incorporating green hydrogen into established energy systems that can help to realize net zero emissions targets It inspires innovation by detailing the experiences of real life case studies and presenting forward looking viewpoints that make collaboration between various sectors possible all towards embracing renewable energy solutions on a global scale Covering

topics such as hydrogen power marketing strategies and public education campaigns this book is an excellent resource for environmental advocates sustainability practitioners policymakers manufacturers industry leaders professionals researchers scholars academicians and more Advances In 3d Integrated Circuits And Systems Hao Yu, Chuan Seng Tan, 2015-08-28 3D integration is an emerging technology for the design of many core microprocessors and memory integration This book Advances in 3D Integrated Circuits and Systems is written to help readers understand 3D integrated circuits in three stages device basics system level management and real designs Contents presented in this book include fabrication techniques for 3D TSV and 2 5D TSI device modeling physical designs thermal power and I O management and 3D designs of sensors I Os multi core processors and memory Advanced undergraduates graduate students researchers and engineers may find this text useful for understanding the many challenges faced in the development and building of 3D integrated circuits and systems

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web the proteins from the recessive allele a did not function as effectively and thus did not produce green pigment in the alligator s scales however if the alligator had both recessive alleles for green pigment the scales would well be green thus

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web a recessive gene will remain dormant unless it is paired with another recessive gene allele is only expressed if the individual has two copies and does not have the dominant allele of that gene

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web which of the following describes recessive inheritance one copy of the allele will express the physical trait two copies of the allele are needed to express the physical trait

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web you either have rh positive rh blood or rh negative rh blood the gene for rh negative blood is recessive so only when you inherit both recessive genes would you have the rh negative phenotype fig 3 figure 3 table depicting types of blood and antigens associated source wikimedia com heredity facts

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